Octagon Satellite PLL LNB with 10 MHz Reference Input

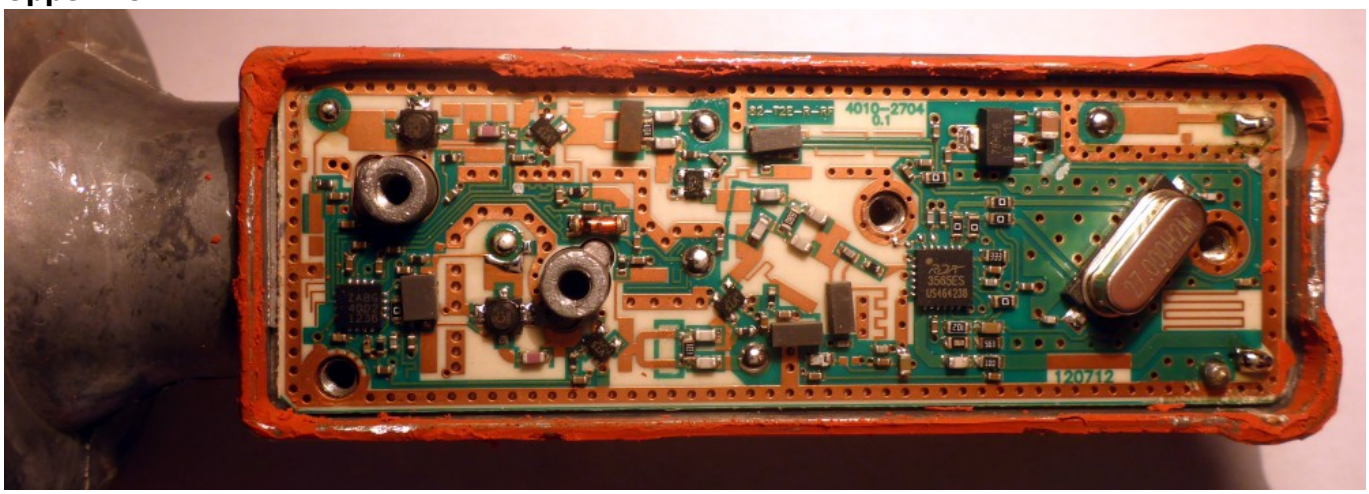
For some years now, Octagon manufactures cheap LNBs for satellite TV reception which use an integrated PLL synthesizer. The required LO frequency is generated from a 27 MHz crystal. In contrast to DRO-based designs, these LOs show much better stability and lower phase noise. These properties make those LNBs suitable for observations in the SSB/CW regions (including beacon frequencies) of the 10 GHz amateur radio bands. Any IF receiver supporting 618 MHz can be used for reception, including the cheap RTL SDR dongles.

Problem statement: Even though frequency stability and accuracy are quite good already, the internal LO still drifts somewhat up and down with temperature. It would be desirable to lock the PLL to an external reference oscillator to remedy this drift.

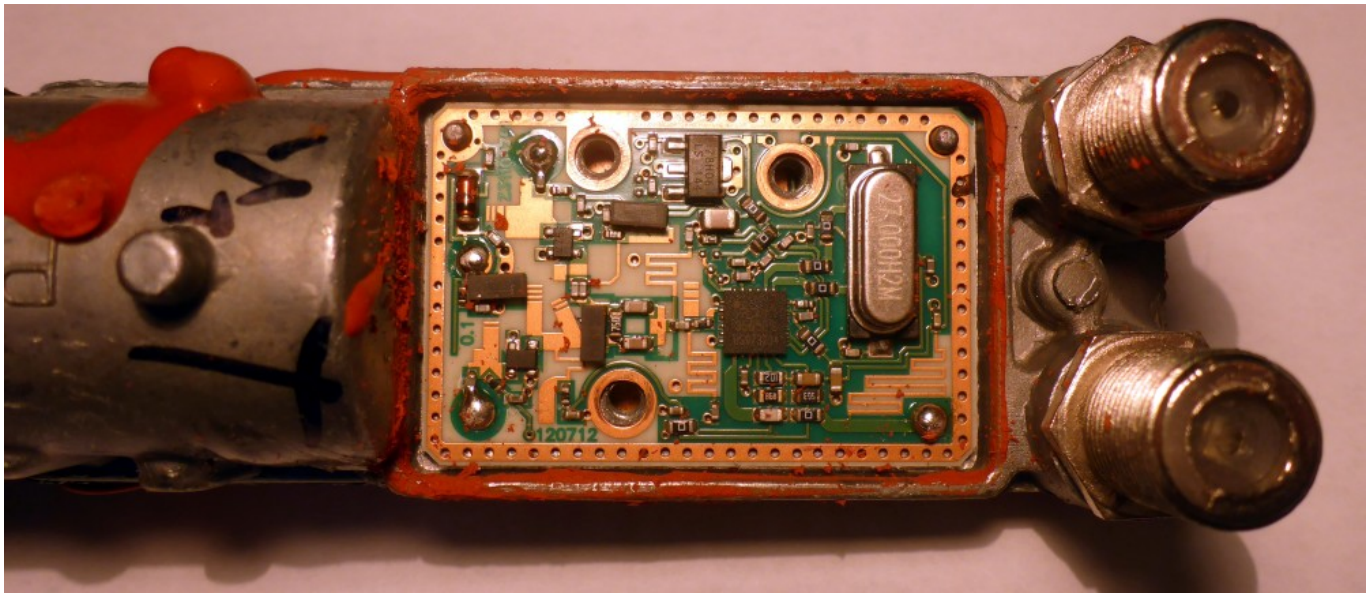
Construction

The dual LNB consists of two separate PCBs. The upper PCB contains the whole 10 GHz frontend for both polarizations and one of the two downconverters (including PLL LO, mixer and IF). The lower PCB only containts a second downconverter. Two type F connectors give access to the independent downconverter outputs.

Upper PCB:



Lower PCB:



Horizontal and vertical polarization use separate front ends, consisting of an LNA and one additional amplifier. Power splitters distribute the amplified signal to the two downconverters. These contain one further amplifier stage per polarization, whose supply voltages are enabled according to the selected polarization. A combiner is used to add the two amplifier outputs (of which only one is active at any time), its output is routed to the RDA3565ES.

The DC voltages from both IF ports used to supply the corresponding downconverters are regulated to 6 volts and additionally combined via diodes to supply the common front end. This way the front end is powered as soon one of the two IF ports delivers DC power.

Between the two PCBs, the following 'vias' exist (position indications according to picture of lower PCB):

- GND - upper left
- 10 GHz input H - upper left
- 10 GHz input V - lower left
- Vcc (5,3V) - center left
- IF output - lower right
- GND - upper right

Implementation

The lower PCB is removed and is substituted by the PLL PCB. Using the second - now unused - F connector, the 10 MHz reference can be supplied. The upper PCB is reused completely. The only required modification there is the removal of the original 27 MHz crystal and connecting the 27 MHz PLL output instead.

Sebastian developed a replacement PCB for the second downconverter. Design files can be downloaded here:

- **Version 2:**
  - Schematic: Eagle, PDF
  - Layout: Eagle
  - Digikey Cart:

BOM

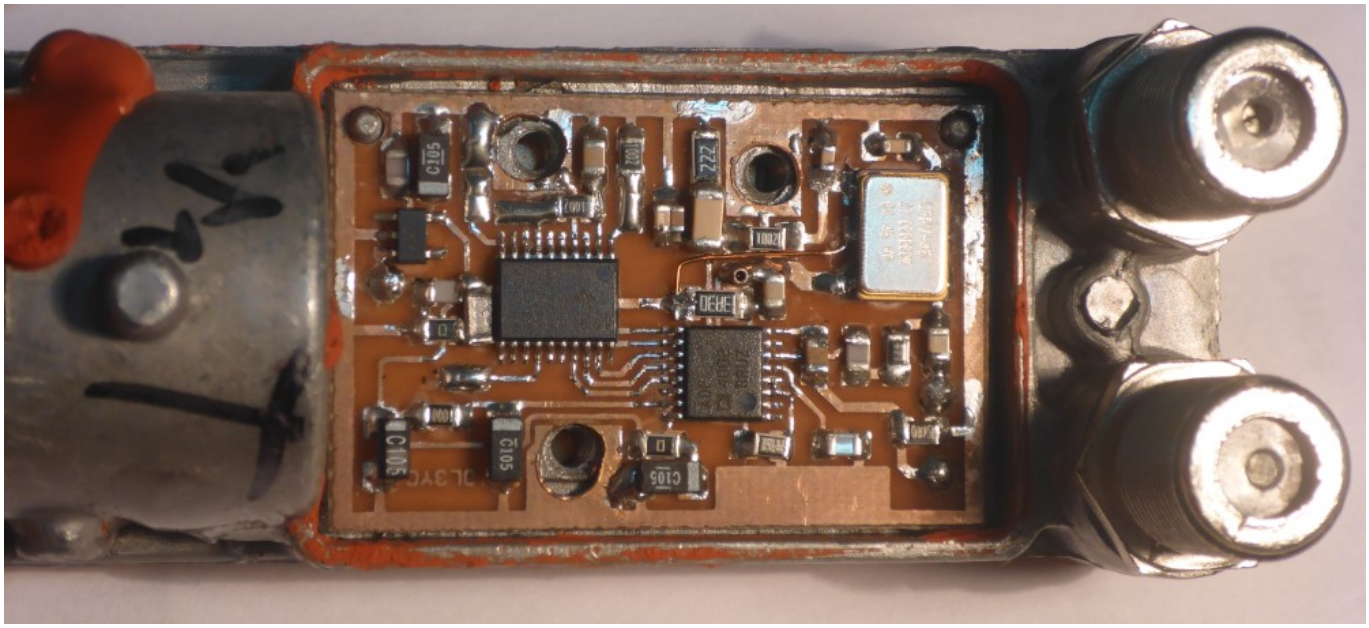
- Sofware:

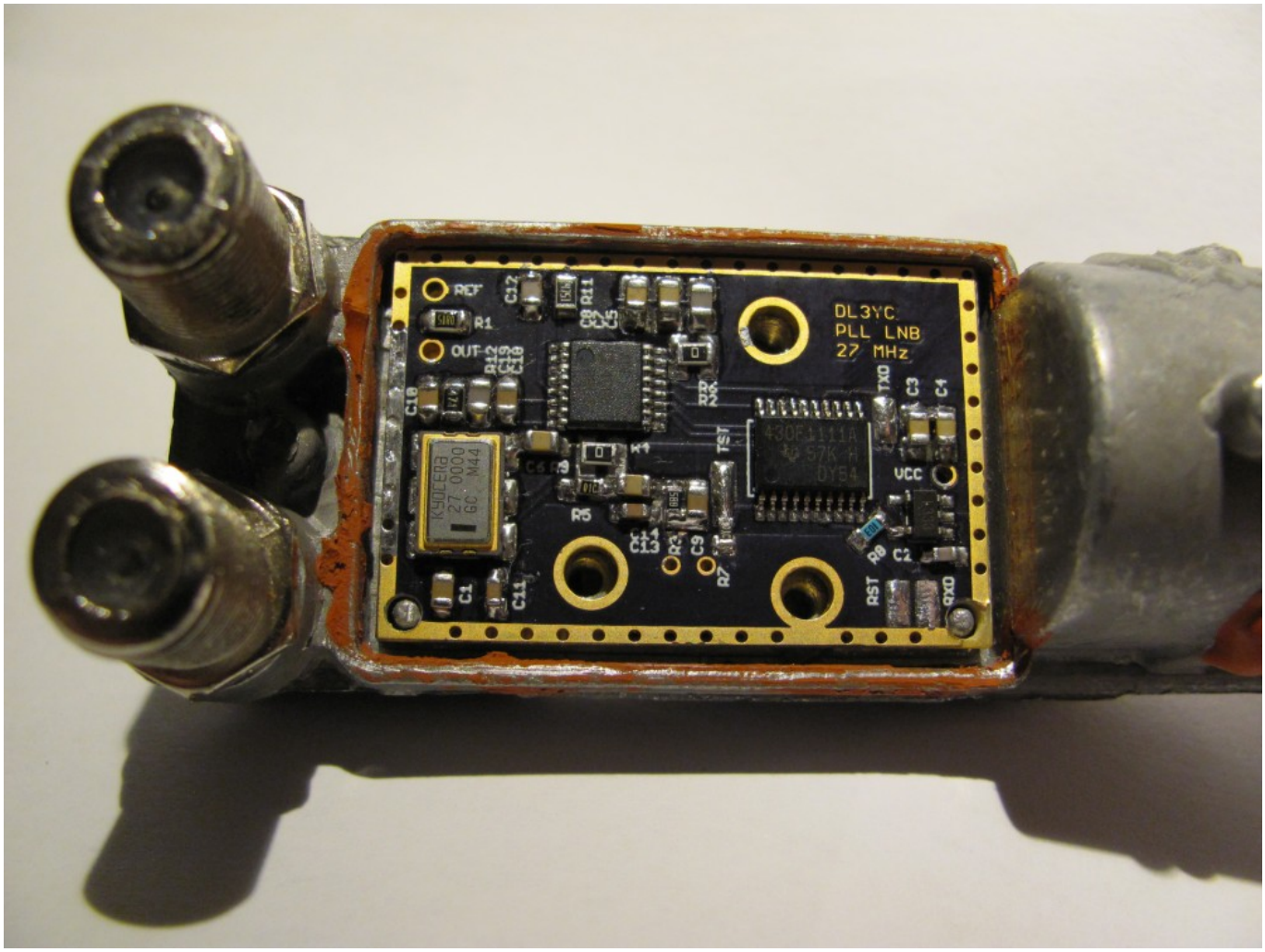
Source
HEX 25 MHz
HEX 27 MHz

- **Version 1:**
  - Schematic: Eagle, PDF
  - Layout: Eagle
  - Sofware: ZIP

For Version 2, the mounting holes positions were fixed and components rearranged in a way that allows reuse of the original cover.

Picures of the hardware (Version 1 and Version 2) instead of the second downconverter:

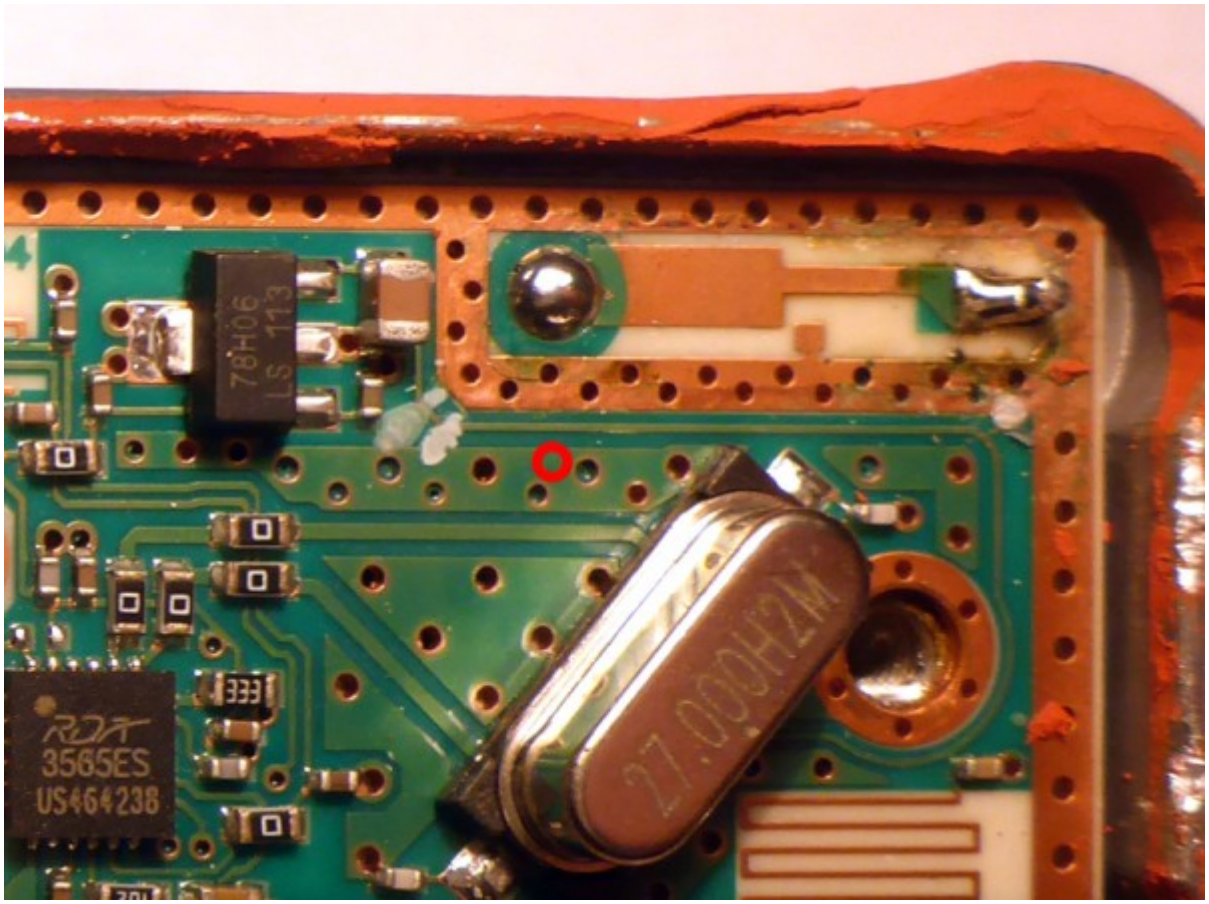




The MSP430F1111 programs the ADF4002 PLL registers and locks the 27 MHz VCXO to the supplied 10 MHz reference input. After successful programming approximately 1.7 V can be measured on the VCXO tuning line.

To make the locked 27 MHz available on the upper PCB, one of the already existing pre-tapped holes can be used. For the hole itself, a 3.2 mm drill should be used. The upper PCB is drilled with a smaller drill, when done right with the hole ending up in a piece of ground plane near the crystal.

Caution: While drilling the case take care NOT to drill through the upper PCB, because a trace on the upper side might get damaged. Use a 1 mm drill bit for the PCB itself and drill through the marked spot:



One of the 'vias' that were gained during the disassembly can be reused and guides the 27 MHz signal upwards, where it can be connected to the nearest pad of the crystal. Be sure to check for short circuits after the modification.